Heavy Ion

Test Summary for the

National LVDS Line Drivers and Receivers

Test Date: February, 1997

Test Location: BNL, NY

Prepared By: NASA/GSFC (R. Katz)

Summary Date: April 23, 1997

Devices Tested: DS90C31 (Transmitter), DS90C32 (Receiver)

DUT Description

From National Semiconductor Literature:

> The DS90C31 is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 155.5 Mbps (77.7 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.
>
> The DS90C31 accepts TTL/CMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition the driver supports a TRI-STATE function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 11mW typical.
>
> The DS90C031 and companion line receiver (DS90C32) provide a new alternative to high power pseudo-ECL devices for high speed point-to-point interface applications.

Some key characteristics:

+/- 350 mV differential voltage; this drastically decreases power in the load resistance.
400 pSec maximum differential skew (5V, 25°C)
3.5 nSec maximum propagation delay
pin compatible with 26C31/26C32 family - note different signalling levels though.
Another key difference from RS-422 is the inability to use these devices for power switching subsystems.
typical rise/fall times of 0.35 nSec!
CMOS epi device with a p-type substrate.

Test Circuit Description

A single DUT card was used to test both the DS90C31 and the DS90C32 devices. The devices were configured in a loop of 4 transmitter-receiver pairs. The input was programmed by the test equipment and remained static over the course of the test. The output was monitored in two ways: first, the output of the loop was directly monitored by the test equipment to ensure that all of the devices were functional; second, the output of the last receiver was fed into the clock input of a 54AC109 configured in a ‘T’ flip-flop mode. This permitted the detection and counting of transient errors since this configuration eliminates the need for a high bandwith link out of the vacuum chamber. The DUT card had a controlled impedance of 100 ohms. The DUTS and terminating resistors were all surface mount devices. The basic schematic is shown in Figure 1.

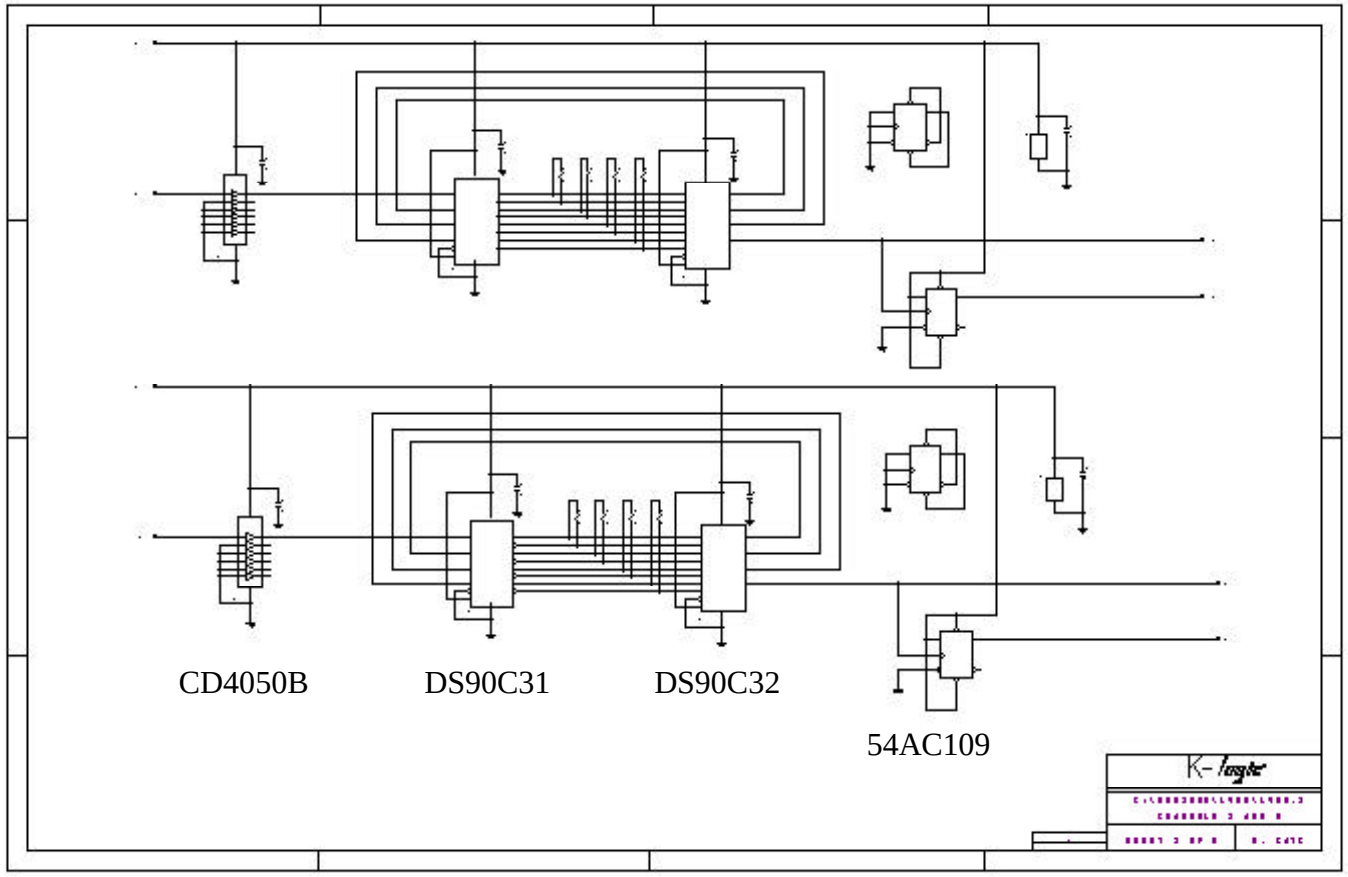

Figure 1: DUT Circuit

DS90C31 Transmitter Test Results

Two devices were tested (S/N 001 and S/N 003) and were exposed to Nickel ions at various angles with LET's ranging from 27.5 to 56.8 MeV/mg/cm^2. All tests were run at V_{CC} = 5.5VDC. A standard fluence of 10^7 ions/cm^2 was used for all runs, except when the run was terminated because of a latchup condition. At an LET of 27.5 MeV/mg/cm^2 the device latched up for 2 out of the 5 runs. Transient upsets were recorded when the device was biased with a logic '0'. For two runs, each with a fluence of 10^7 ions/cm^2 and the device biased with a logic '1', no upsets were seen. Upsets were seen with higher LETs but the data was contaminated by the device latching up. LVDS DS90C31 latchup data is shown in Figure 2; upset data is shown in Figure 3.

Discussions with the manufacturer are ongoing concerning the latchup of the transmitter device. It is planned that additional devices will be tested in May of 1997.

DS90C32 Receiver Test Results

Three devices were tested (S/N 001, S/N 002, and S/N 003) and were exposed to Chlorine, Nickel, and Bromine ions at various angles with LET's ranging from 17.1 to 77.3 MeV/mg/cm^2. All tests were run at either V_{CC} = 4.5VDC or 5.5VDC. A standard fluence of 10^7 ions/cm^2 was used for all runs. There were no latchups detected for any run. Transient upsets were recorded when the device was biased with either a logic '0' or a logic '1', with the logic '1' state appearing slightly harder. The transient upset threshold for these devices is approximately 20 MeV/mg/cm^2. LVDS DS90C32 upset data is shown in Figure 4.

LATCH-UP CURRENTS (representative)

Run #	Nominal Current	Latch-up Current	Delta
LVT1R20	20.37mA	55.64-56.49mA	35.7mA
LVT1R22	20.33-20.4mA	55.9-56.4mA	35.8mA

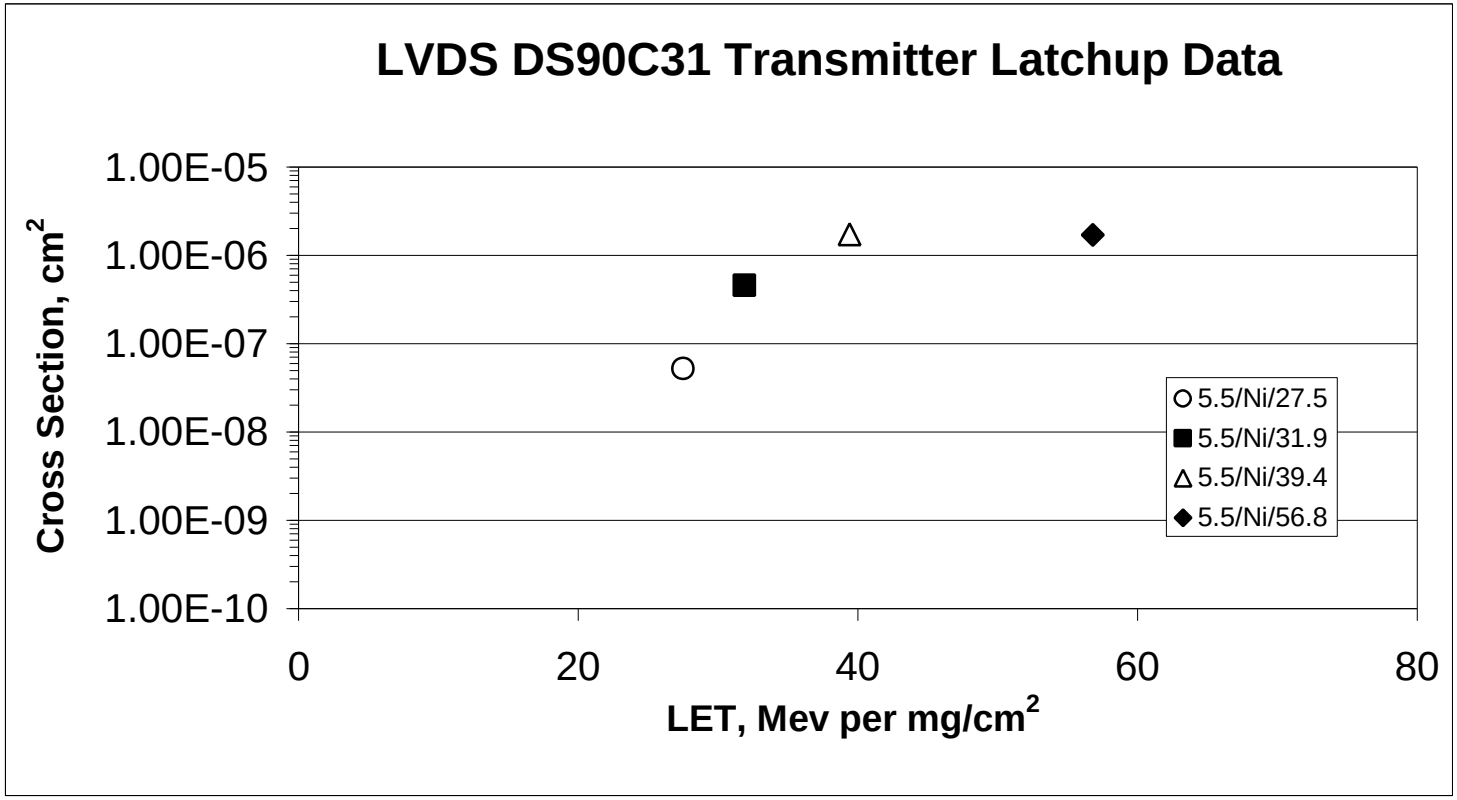

Figure 2: LVDS Transmitter Latchup Data

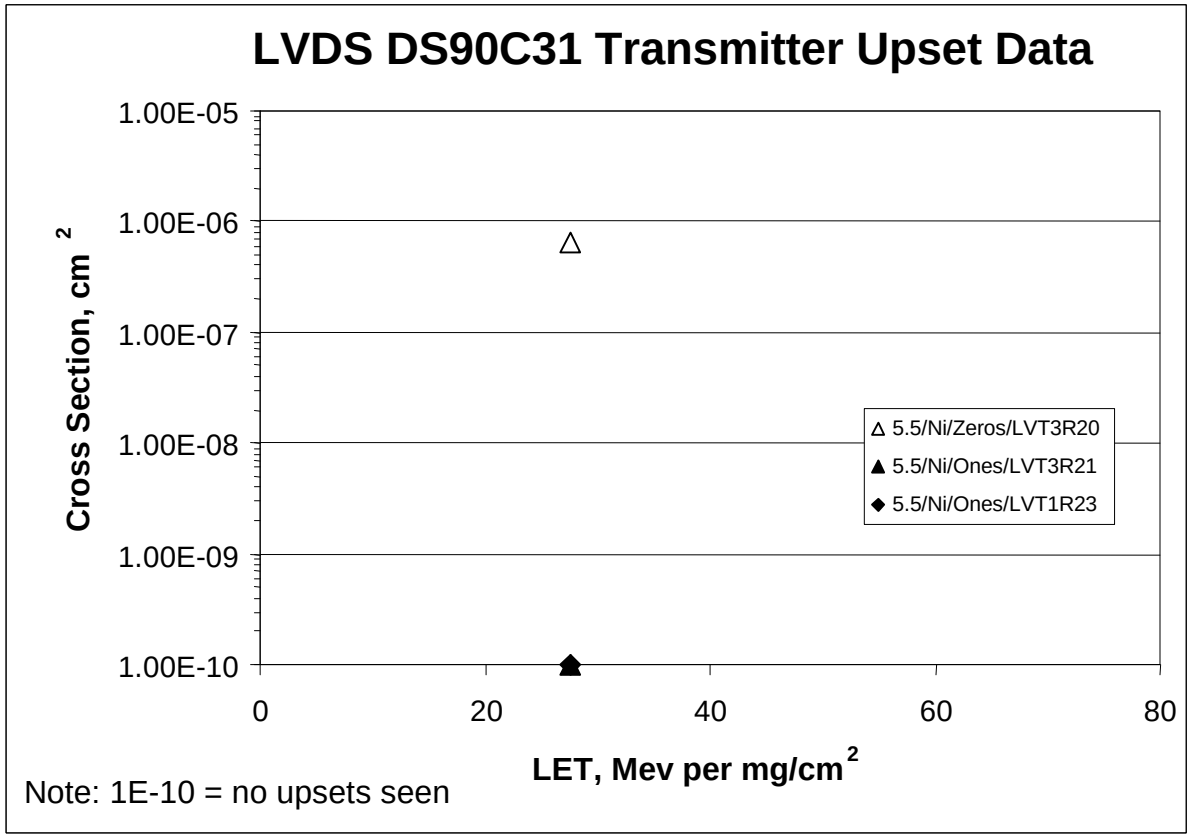

Figure 3: LVDS Transmitter Upset Data

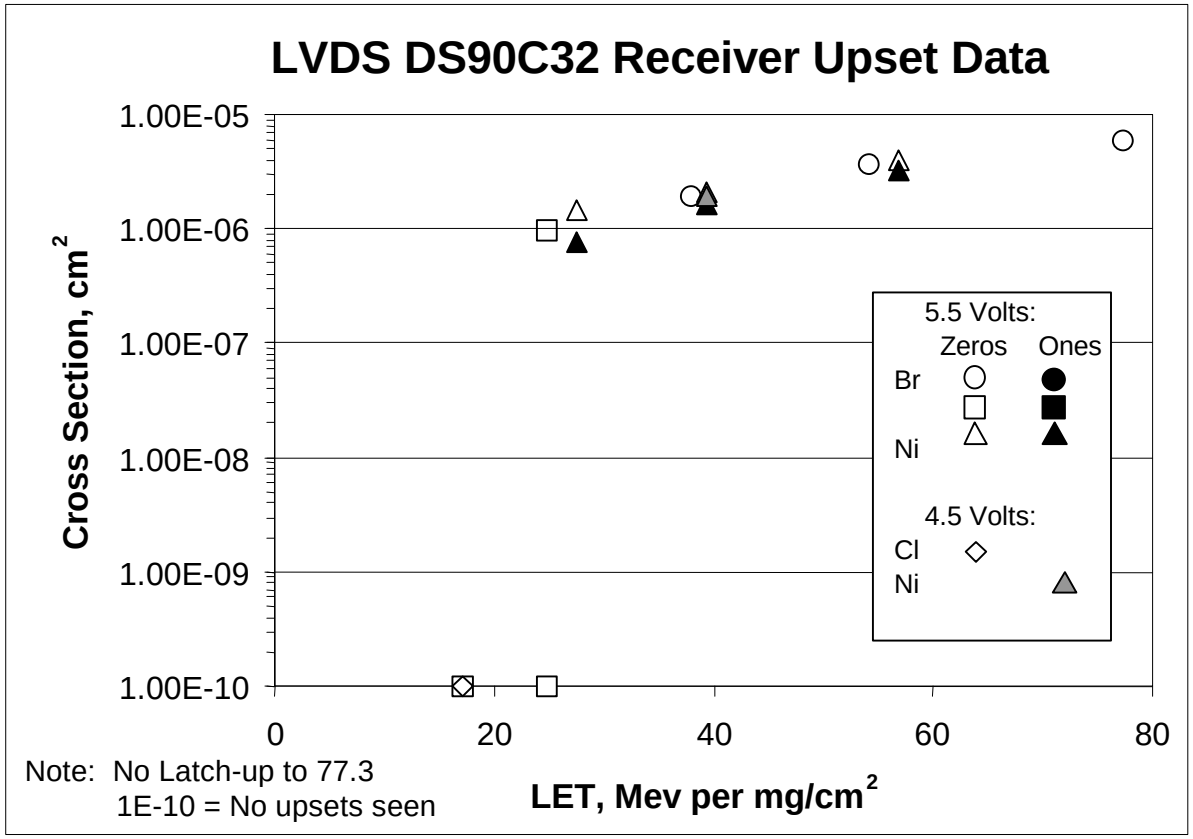

Figure 4: LVDS Receiver Transient Upset Data